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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/710,298	06/30/2004	Wensong Chen	PS-123	4297

23933 7590 05/02/2005

STUART T AUVINEN
429 26TH AVENUE
SANTA CRUZ, CA 95062-5319

EXAMINER	
LE, DON P	

ART UNIT	PAPER NUMBER
2819	

DATE MAILED: 05/02/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/710,298	CHEN ET AL.	
	Examiner	Art Unit	
	Don P. Le	2819	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 June 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *19 and 20* is/are allowed.

6)☒ Claim(s) *1-8 and 11-18* is/are rejected.

7)☒ Claim(s) *9, and 10* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 4/25/05
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1, 2, 4 and 12-18 are rejected under 35 U.S.C. 102(b) as being anticipated by Shigehara (US 6,194,952).

3. With respect to claims 1 and 12, figure 23 Shigehara of discloses an apparatus comprising:

a bus-switch transistor (N1), having a gate driven by an enable signal (EN), a drain connected to a first input (A), and a source connected to a second input (B);

an isolated well under the bus-switch transistor, the isolated well isolated from a supply, the supply being a power source or a ground;

a well tap for electrically connecting to the isolated well;

a first well-shorting transistor (N1N), having a gate driven by the enable signal, a drain connected to the first input, and a source connected to the well tap;

a second well-shorting transistor (N2N), having a gate driven by the enable signal, a drain connected to the second input, and a source connected to the well tap; and

a biasing transistor (N2), formed outside the isolated well, responsive to the enable signal or to an inverse of the enable signal, having a channel between the well tap and the supply that conducts current when the enable signal turns off the bus-switch transistor,

whereby the isolated well is shorted to the first and second input when the bus-switch transistor is turned on.

4. With respect to claim 2, figure 23 of Shigehara discloses the circuit a parasitic drain-to-well capacitor of the bus-switch transistor (N1) is shorted by the first well-shorting transistor when the enable signal turns on the bus-switch transistor;

wherein a parasitic source-to-well capacitor of the bus-switch transistor is shorted by the second well-shorting transistor when the enable signal turns on the bus-switch transistor,

whereby parasitic source-to-well and drain-to-well capacitors are shorted to reduce input capacitance.

5. With respect to claims 4, 13 and 14, figure 23 of Shigehara discloses a metal line connecting the biasing transistor to the well tap (Pw to well).

6. With respect to claim 15, figure 23 of Shigehara discloses first and second inverters (INV1, INV2).

7. With respect to claim 16, figure 23 of Shigehara discloses the biasing transistor means has a gate that receives the inverse enable signal (VGP), while the bus-switch transistor means, the first well-shorting transistor means, and the second well-shorting transistor means each have a gate receiving the enable signal (VGN).

8. With respect to claim 17, figure 23 of Shigehara discloses the biasing transistor an n-channel transistor (N2), wherein the first and second well-shorting transistor means are

n-channel transistors (N1N, N2N), wherein the supply voltage is a ground, and wherein the floating well means is a P-well.

9. With respect to claim 18, figure 1 of Shigehara discloses the biasing transistor means is a p-channel transistor (P2),

wherein the bus-switch transistor means is a p-channel transistor (P1),

wherein the first and second well-shorting transistor means are p-channel transistors (P1P, P2P),

wherein the supply voltage is a power supply, and wherein the floating well means is an N-well.

Claim Rejections - 35 USC § 103

10. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

11. Claims 3, 5-8 and 11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Shigehara (US 6,194,952).

12. With respect to claims 3 and 5, the apparatus of Shigehara does not specifically disclose the doping concentration of the isolated well as claimed by applicant. However, it is notoriously well known in the art that doping of MOSFET to obtain a specific electrical characteristic. It would have been obvious to one of ordinary skill of art at the time the invention was made to

have doped the isolated well at least two orders of magnitude less than doping concentration of the source and the drain to obtain a desired response as a design choice.

13. With respect to claim 6, figure 23 of Shigehara discloses the biasing transistor (N2) has a drain connected to the well tap and a source connected to the supply.

14. With respect to claim 7, figure 23 of Shigehara discloses the bus-switch transistor, the first well-shorting transistor (N1N), and the second (N2N) well-shorting transistor are n-channel transistors and wherein the isolated well is a P-well.

15. With respect to claim 8, figure 23 of Shigehara discloses the supply is the ground.

16. With respect to claim 11, figure 1of Shigehara discloses a similar circuit using P-channel switch (P1) and two p-channel shorting transistors (P1P, P2P).

Allowable Subject Matter

17. Claims 19 and 20 are allowed.

18. Claims 9 and 10 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

19. The following is an examiner's statement of reasons for allowance:

With respect to claims 9 and 19, the prior art does not teach a second well.

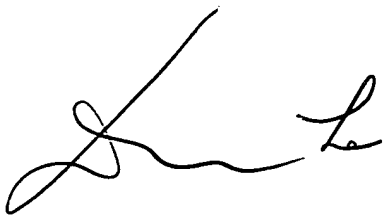
Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

20. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Don P. Le whose telephone number is 571-272-1806. The examiner can normally be reached on 7AM - 5PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael J. Tokar can be reached on 571-272-1812. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

4/25/2005



DON LE
PRIMARY EXAMINER